# ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, OAKLAND UNIVERSITY ECE-2700: Digital Logic Design

### **Student Honor Pledge:**

All work submitted is completed by **Quiz 2** me directly without the use of any unauthorized resources or assistance (February 9<sup>th</sup> @ 5:30 pm) Initials: \_\_\_\_\_

## PROBLEM 1 (40 PTS)

• Complete the following table:

| REPRESENTATION |                    |                |                |
|----------------|--------------------|----------------|----------------|
| Decimal        | Sign-and-magnitude | 1's complement | 2's complement |
|                | 11010              |                |                |
|                |                    |                | 0110           |
|                |                    | 1010           |                |
| -7             |                    |                |                |

• Convert the following decimal number to its 2's complement representation: -7.75 (5 pts)

## PROBLEM 2 (20 PTS)

• Perform the following operation in the 2's complement system, i.e., provide the summands and the result in 2's complement representation (<u>indicate the carries</u>). Use the minimum number of bits to represent both the summands and the result so that the overflow bit is 0.

✓ -14 + 21

## PROBLEM 3 (40 PTS)

• Complete the timing diagram of the circuit shown below:  $y = y_3y_2y_1y_0$ ,  $x = x_1x_0$ 

